CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Original) A method of analyzing a design in a high level modeling system that supports unidirectional flow, comprising:
selecting a link represented by at least a portion of the design;
determining a directionality for the link selected; and
in response to determining the link to be bidirectional, emulating the link in the design using first and second unidirectional links.

2. (Original) The method of claim 1, in which the emulating represents the second unidirectional link in opposite data-routing orientation relative to the first unidirectional link.

3. (Original) The method of claim 2, further comprising:
simulating signal excitation on at least a portion of the design, the portion to model a circuit; and
determining results from the simulating signal excitation.

4. (Original) The method of claim 3, in which the simulating and determining results are performed using the emulated first and second unidirectional links.

5. (Original) The method of claim 1, further comprising:
responsive to determining a tap interconnect represented by another portion of the design to be coupled to the bidirectional link, emulating the tap interconnect in the design of the circuit system model using at least one unidirectional input line and a unidirectional output line.

6. (Original) The method of claim 5, further comprising emulating the unidirectional output line in parallel relationship to the at least one unidirectional input line.

7. (Original) The method of claim 5, further comprising:
simulating signal excitation of at least a portion of the design with the emulated first and second unidirectional links and the emulated tap interconnect; and
responsive to the simulating signal excitation, emulating a tri-state buffer in series with the unidirectional input line.

8. (Original) The method of claim 5, further comprising simulating operation of the design with the emulated first and second unidirectional links and emulated tap interconnect, the simulating to comprise:
emulating a tri-state buffer in series with the unidirectional input line.

9. (Original) The method of claim 8, the simulating to further comprise:
determining an absence of an input signal on each of the first and second unidirectional links; and
conditioning an enablement of the emulated tri-state buffer on determining the absence of an input signal on each of the first and the second unidirectional links.

10. (Original) The method of claim 5, further comprising:
simulating operation of at least a portion of the design with the emulated first and second unidirectional links and emulated tap interconnect, the design to model a circuit system, and the simulating to comprise:
representing a signal on each of the unidirectional output line and the outputs of the first and second unidirectional links responsive to determining a signal being represented at the at least one unidirectional input line.

11. (Original) The method of claim 10, the simulating further comprising:
representing a signal on the unidirectional output line and the output of the first/second unidirectional link responsive to a signal being represented at the input of the second/first unidirectional link.

12. (Original) The method of claim 11, the simulating further comprising:
identifying a collision event responsive to determining a signal represented at the input of either one of the first and second unidirectional links when representing a signal presented to the unidirectional input line.

13. (Withdrawn) A method of testing a design in a high level modeling system of unidirectional elements, comprising:
identifying a bus-block;
representing the bus-block within the design and associated with a bus, and
interfacing a tap to the bus in the design via the bus-block.

14. (Withdrawn) The method of claim 13, in which the representing and interfacing comprise:
representing the tap with unidirectional input and output tap lines coupled to the bus-block;
substituting for a first port of the bus a first representation of unidirectional, oppositely directed, input and output lines as the first port coupled to the bus-block; and
substituting for a second port of the bus a second representation of unidirectional, oppositely directed, input and output lines as the second port coupled to the bus-block.

15. (Withdrawn) The method of claim 14, in which the representing the bus-block within the design further comprises representing the bus-block as being disposed serially with and between the first and second ports of the selected bus of a system model.

16. (Withdrawn) The method of claim 14, further comprising:
associating rules with the bus-block,
the rules to simulate propagation of signals among the input and output tap lines, the first port and the second port during testing of the design.

17. (Withdrawn) The method of claim 16, in which the associating the rules with the bus-block comprises:
storing a conditional test sequence in memory;
performing the conditional test sequence dependent on performance of a simulating operation of the bus-block;
the test sequence to comprise representing a first signal on all output lines responsive to determining a second signal being presented to the input tap line.

18. (Withdrawn) The method of claim 17, in which the first signal is different from the second signal.

19. (Withdrawn) The method of claim 18, further comprising generating the first signal representative of the second signal.

20. (Withdrawn) The method of claim 16, in which the associating the rules with the bus-block comprises:
storing a conditional test sequence in memory;
performing the conditional test sequence dependent on performance of a simulating operation of the bus-block;
the test sequence to comprise representing an output signal at each of the output tap lines, and the output lines of the first port and the second port responsive to determining a signal being represented at the input line for the tap.

21. (Withdrawn) The method of claim 20, further comprising relating the output signal to the signal represented at the input line.

22. (Withdrawn) The method of claim 20, the conditional test sequence to further comprise conditioning the presentment of the output signal upon determining the absence of signal(s) at each of the input lines of the first and the second ports.

23. (Withdrawn) The method of claim 22, the conditional test sequence to further comprise identifying a collision responsive to determining representation of a signal at the input line for the tap when a signal is represented at the input line of at least one of the first and second ports.

24. (Withdrawn) The method of claim 23, further comprising simulating operation of at least a portion of the design.

25. (Withdrawn) The method of claim 24, in which the simulating comprises testing at least a portion of the design using a system-level, computer aided analysis system.

26. (Withdrawn) The method of claim 25, further comprising displaying results of the testing.

27. (Original) A computer readable medium having stored thereon computer readable instructions to perform, when executed by a computer in a high level modeling system supporting unidirectional data flow, analysis of at least a portion of a system model by a method comprising:

retrieving from memory data representative of a system model;

determining if a link represented by at least a portion of the system model is to be bi-directional;

based on the determining of the link to be bidirectional, modifying the system model by using two separate and oppositely directed, unidirectional links for emulating the bi-directional link.

28. (Original) The medium of claim 27, in which the method further comprises:
simulating signal excitation of at least a portion of the system model modified with the two separate unidirectional links; and
recording responses from the simulating.

29. (Original) The medium of claim 27, in which the method further comprises:
realizing at least a portion of the system model, the realizing to comprise:
representing first and second, oppositely directed data-routing, unidirectional lines for a tap to interconnect the bidirectional link,
representing a tri-state buffer in series with the first one of the unidirectional lines for the tap, and
representing the tri-state buffer to drive the second one of the unidirectional lines for the tap and the two separate unidirectional links.

30. (Original) The medium of claim 29, in which the method further comprises:
determining a first signal represented at the first unidirectional line for the tap; and
responsive to the determining of the first signal at the first unidirectional line for the tap, representing a second signal on the second unidirectional line for the tap and the two separate unidirectional links.

31. (Original) The medium of claim 30, in which the method further comprises:
identifying a collision responsive to determining a signal being represented at an input of either one of the first and second unidirectional links when determining a signal represented at the first unidirectional line for the tap.